

 Drafts BRS: Pending Active

- L4: (65482) split near gate near flash near memory or EEPROM\$1 or (electrically near erasable ne...
- L3: (65492) split near gate near flash near memory or EEPROM\$1 or (electrically near erasable ne...
- L5: (946) 3 and floating near gate near insulator\$3
- L6: (231) 3 and floating near gate near insulator\$3 and control near gate and space\$3

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- S1: (65482) split near gate near flash near memory or EEPROM\$1 or (electrically near erasable ne...
- S2: (64549) split near gate near flash near memory or EEPROM\$1 or split-gate near memory or split...
- S4: (1) S3 and intergate near insulator
- S3: (601) S2 and (floating near gate) and control near gate and space\$1 and gate near insulator\$3...
- S5: (74) S1 and intergate near insulator\$3

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3 and floating near gate near insulator\$3 and control near gate and spacer

	Document ID	Issue Date	Pages	Title	Current EP	Current Xref
20	<input checked="" type="checkbox"/> US 20040171243 A1	20040902	20	Method of forming a conductive pattern of a semiconductor device and method of manufacturing a non-volatile semiconductor memory device	438/593	436/585
21	<input checked="" type="checkbox"/> US 20040171217 A1	20040902	21	Method of manufacturing a floating gate and method of manufacturing a non-volatile semiconductor memory device comprising the same	438/257	
22	<input checked="" type="checkbox"/> US 20040152268 A1	20040805	9	Novel method of fabricating split gate flash memory cell without select gate-to-drain bridging	438/266	436/257; 436/258
23	<input checked="" type="checkbox"/> US 20040151021 A1	20040805	14	Nonvolatile memory capable of storing multibit binary information and the method of forming the same	365/149	
24	<input checked="" type="checkbox"/> US 20040135193 A1	20040715	19	Cell structure of EEPROM device and method for fabricating the same	257/315	
25	<input checked="" type="checkbox"/> US 20040132250 A1	20040708	75	Preventing dielectric thickening over a gate area of a transistor	438/264	257/E21.682; 257/E27.103; 257/E29.129
26	<input checked="" type="checkbox"/> US 20040132248 A1	20040708	11	Flash memory cell and method for fabricating the same	438/257	257/E21.309; 257/E21.689; 257/E29.129
27	<input checked="" type="checkbox"/> US 20040130947 A1	20040708	31	Flash memory with trench select gate and fabrication process	365/185.05	365/51
28	<input checked="" type="checkbox"/> US 20040119112 A1	20040624	12	Multi-level memory cell with lateral floating spacers	257/316	257/E21.309; 257/E21.689; 257/E27.081
29	<input checked="" type="checkbox"/> US 20040106259 A1	20040603	12	High coupling split-gate transistor	438/267	257/E21.682; 257/E27.103
30	<input checked="" type="checkbox"/> US 20040105319 A1	20040603	25	METHOD OF MANUFACTURING A SCALABLE FLASH EEPROM MEMORY CELL WITH FLOATING GATE SPACER WRAPPED BY CONDUCTIVE GATE	365/199	257/E21.422; 257/E21.682; 257/E29.306

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